An Analysis on a Pseudo-Differential Dynamic Comparator with Load Capacitance Calibration

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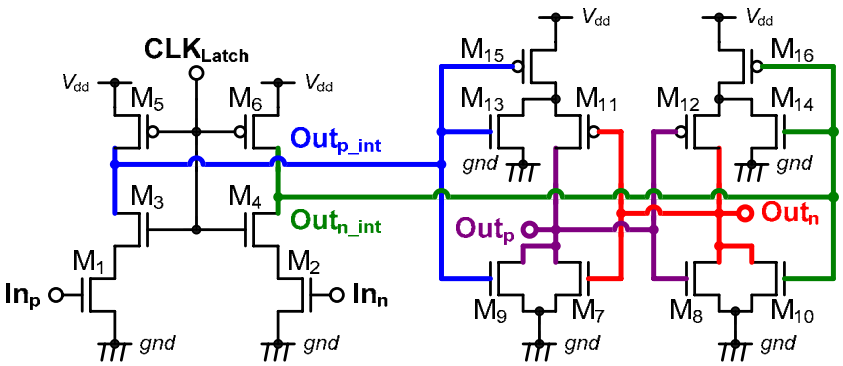
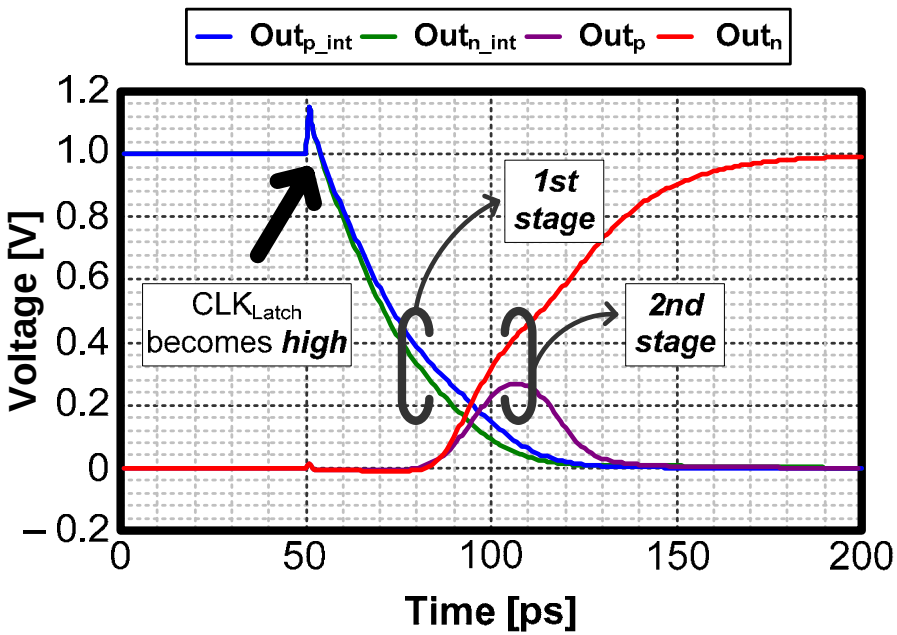
An Analyzed Comparator





- CLK_{Latch} becomes high
  1. Electric charge on the node Out_{int} flows into *gnd*
  2. **Current difference** is determined by input signals
     - The difference is **integrated on Out_{int} and becomes larger as time passes**
  3. The second stage regenerates the voltage difference

Fig. Transient waveform of a comparator **[6], [7]**.

[6] M. Miyahara, *et al.*, *ASSCC*, 2008 **[7] D. Paik, *et al.*, *IEICE Trans. on Fundamentals*, 2010**

Analysis Conditions of a Pre-amplifier

- Process is 90-nm CMOS
- The size of all transistors is 2 μm/100 nm
- To simplify the analysis
  - The rising time of CLK_{Latch} to 1 ps
  - M_3 and M_4 are in the deep triode when CLK_{Latch} is high
    - V_{out_int} can be approximated as the drain voltage of M_1 (or M_2)

$$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C} t$$

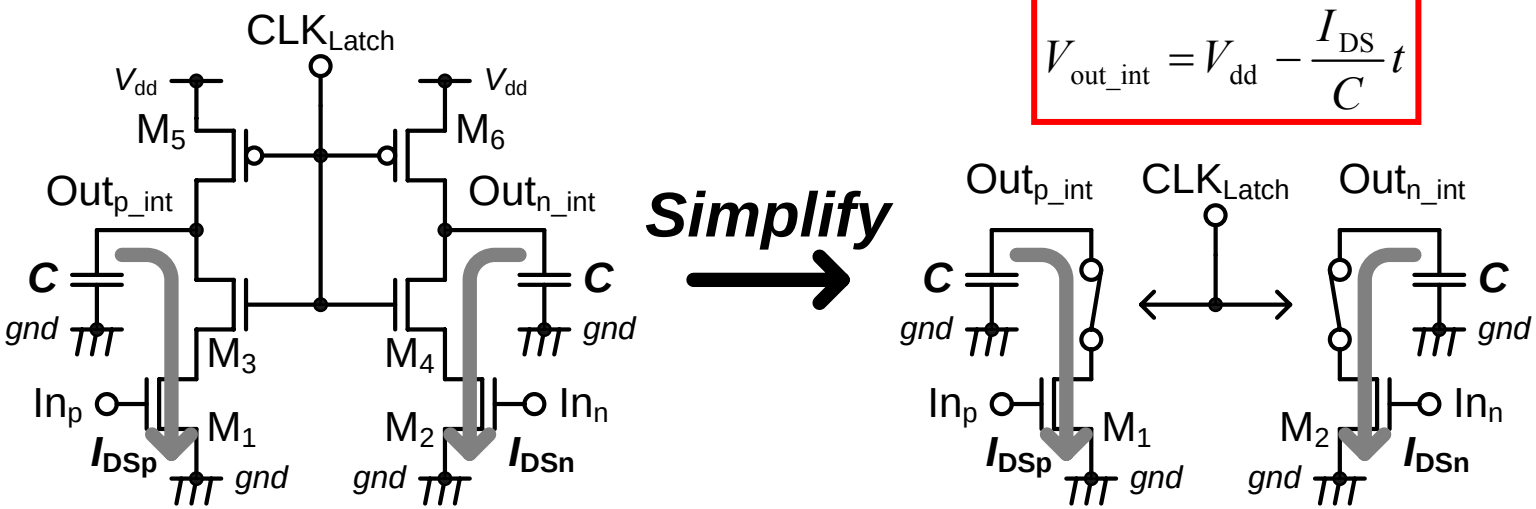


Fig. Simplified schematic of a dynamic amplifier when the CLK_{Latch} is high.

Mismatch Contribution

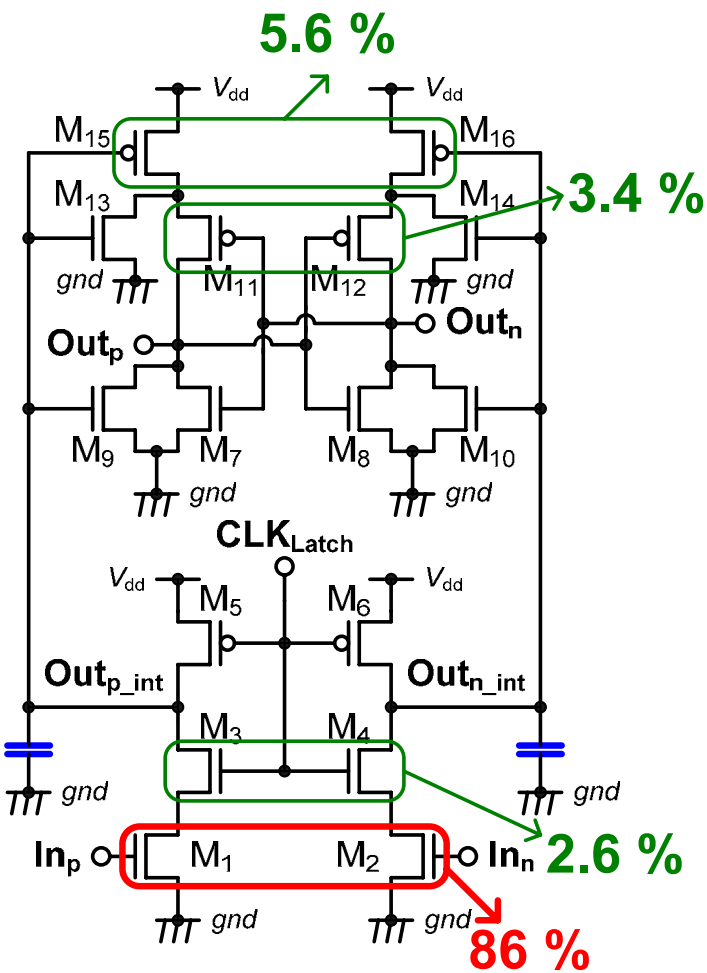


Fig. Mismatch contribution (Remains are 2.4 %).

- Mismatch is **dominated by a pair of input transistors**
  - Mismatch of the second stage is suppressed by the gain of the pre-amplifier
  - I_{DS} is mainly decided by input transistors
    - Mismatch changes I_{DS} and the slew rate of Out_{int} is also varied

$$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C}t \quad \longrightarrow \quad \frac{dV_{out\_int}}{dt} = -\frac{I_{DS}}{C}$$

  - Load capacitance calibration [2], [3] is commonly used to compensate mismatch
    - **To figure out the calibration effect, the gain is required**

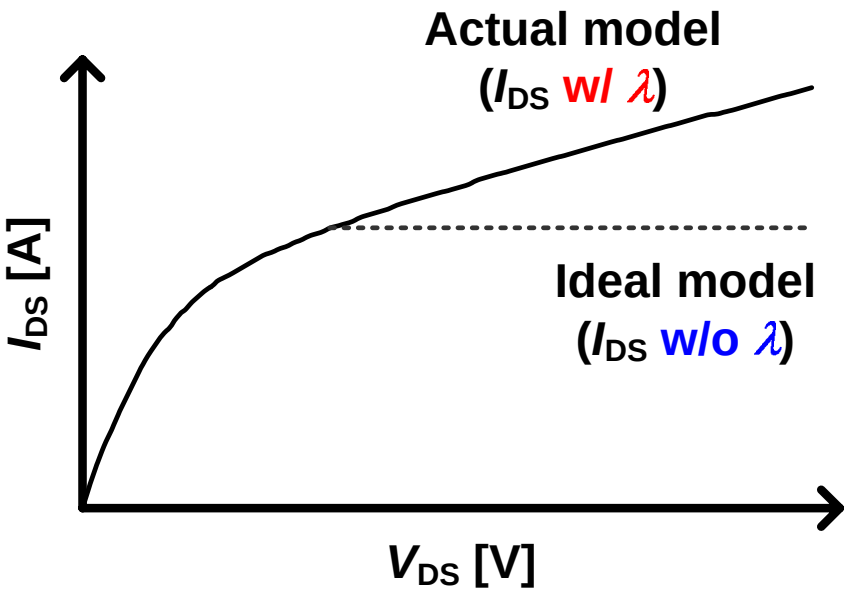
[2] V. Giannini, *et al*., *ISSCC*, 2008 **[3] G. Van der Plas, *et al*., *ISSCC*, 2008**

Channel-Length Modulation

- I_{DS} is affected by the channel-length modulation
  - λ is the channel-length coefficient

$$V_{out\_int} = V_{dd} - \frac{I_{DS}}{C}t$$

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{eff}^2\left(1+\lambda\left(V_{DS}-V_{DS\_sat}\right)\right)$$



- $V_{eff} \equiv V_{GS} - V_{th}$
- V_{DS_sat} = the saturation condition of drain-source voltage (= V_{eff})

Fig. Influence of the channel-length modulation.

Gain of A Dynamic Amplifier

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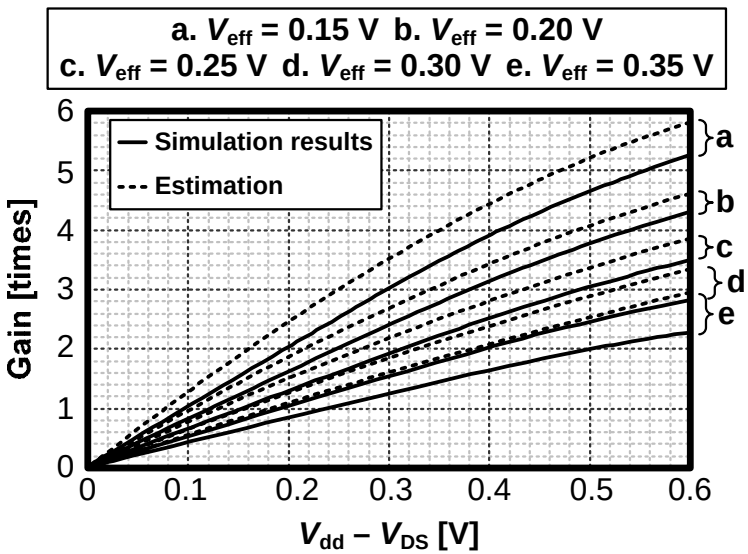
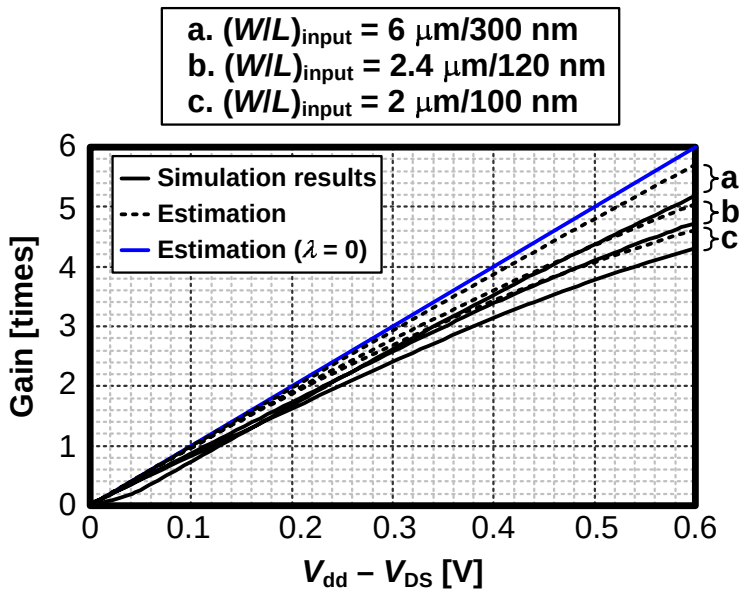
- G_{amp_trans} is satisfied only when $V_{out\_int} \geq V_{eff}$
  - If V_{out_int} falls to V_{eff}, G_{amp_trans} reaches its maximum

$$G_{amp\_trans} = \frac{v_{out}}{v_{in}} = -\frac{\overline{i_{DS}}t}{C} \times \frac{1}{v_{in}} = -\frac{2(V_{dd} - V_{DS})}{V_{eff}} \times \frac{1 + \lambda(V_{DS} - V_{eff})}{1 + \frac{\lambda}{2}(V_{dd} + V_{DS} - 2V_{eff})}$$



(a) various V_{eff}



(b) various channel length when V_{eff} is 0.2 V

Fig. Gain of a pre-amplifier.

Load Capacitance Calibration

- Using binary-weighted PMOS varactors
- By turning on or off PMOS, capacitance is varied
  - Reduce offset voltage

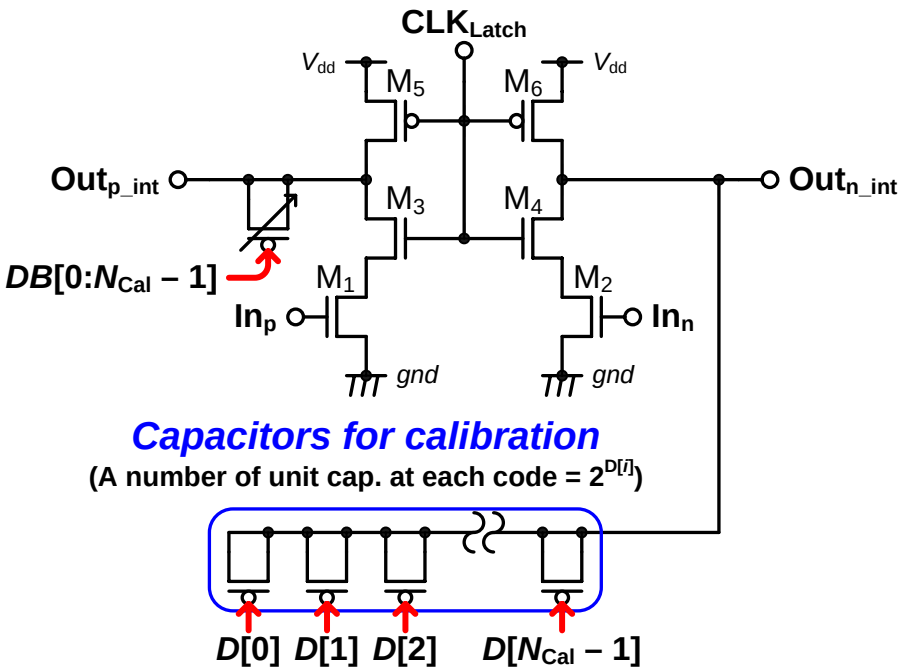


Fig. Load capacitance calibration.

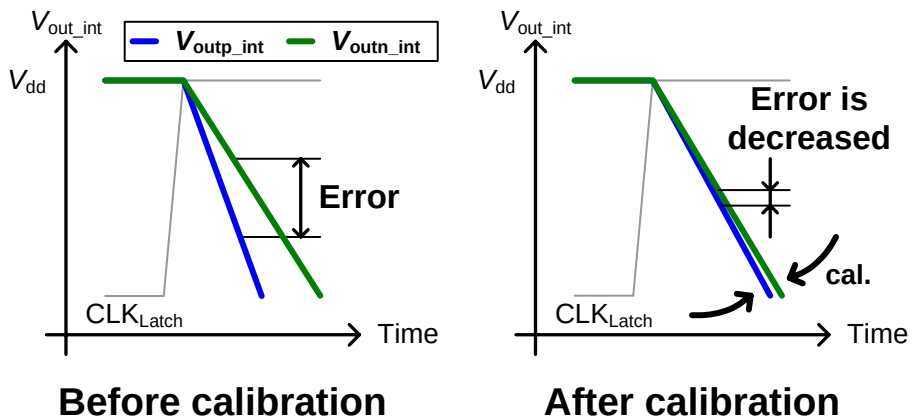


Fig. Error reduction by calibration ($V_{inp} = V_{inn}$).

Input-Referred Compensated Voltage

- **Assumption**
  - Input signal of the second stage is decided when gain reaches its maximum

$$v_{\text{in\_diff\_cal}} = \left(\frac{\mathrm{d}V_{\text{out\_int}}}{\mathrm{d}C}\right)_{\text{input-referred}} \times \Delta C_{\text{cal}}$$

$$= -\frac{V_{\text{eff}}}{C} \times \left(1 + \frac{\lambda}{2}\left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \times \left(N_{\text{Code}} - 2^{N\text{cal}-1}\right) \times \left(C_{\text{on}} - C_{\text{off}}\right)$$

- ($N_{\text{Code}} - 2^{N\text{cal}-1}$): **$\Delta N_{\text{Code}}$** from the middle of calibration code
  N_{Code}: calibration code
  N_{Cal}: calibration resolution
- ($C_{\text{on}} - C_{\text{off}}$): **capacitance difference** of a unit PMOS varactor
  C_{on}: **on** capacitance of a unit PMOS varactor
  C_{off}: **off** capacitance of a unit PMOS varactor

Simulation Results

- Simulation condition
  - 1 LSB = 1.5 mV
  - V_{dd} = 1.0 V and V_{in_com} = 0.5 V
  - Size of a unit varactor is W/L = 600 nm/100 nm

$$\text{Estimation}: \frac{V_{\text{eff}}}{C} \times \left(1 + \frac{\lambda}{2}\left(V_{\text{dd}} - V_{\text{eff}}\right)\right) \times \left(N_{\text{Code}} - 2^{N_{\text{cal}}-1}\right) \times \left(C_{\text{on}} - C_{\text{off}}\right)$$

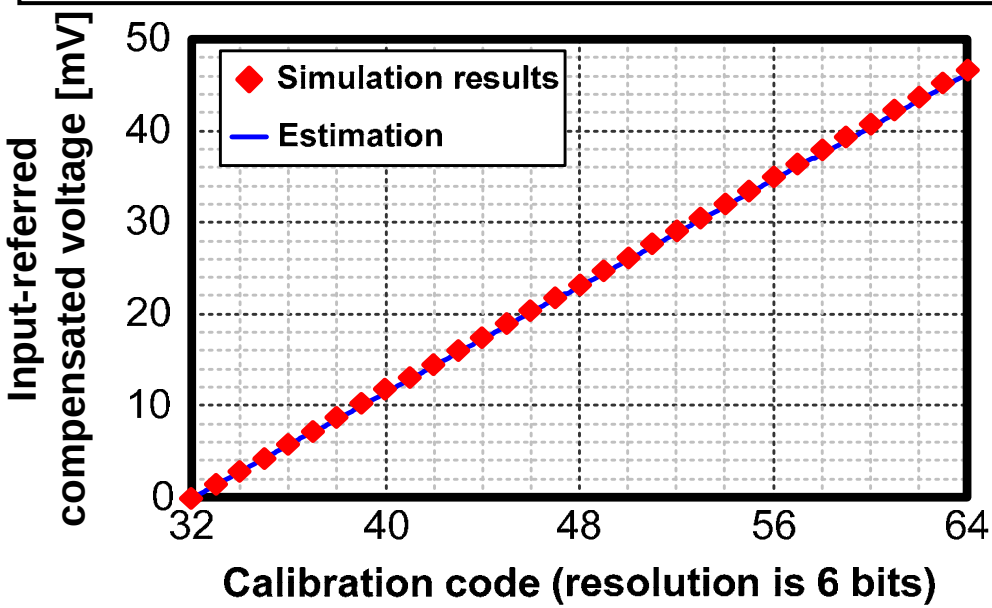


Fig. Input-referred compensated voltage by the capacitance calibration.

PVT Variation

- If **surrounding condition is varied** after compensation, **calibration** accuracy **is degraded**
  - Process is fixed in the factory
  - **Voltage** and **Temperature** should be considered
- **Assumption**
  - An error due to PVT variation, σ_{V_PVT}, is **uncorrelated** with offset after calibration, $\sigma_{V\_offset0}$

$$\sigma^2_{V\_offset} = \sigma^2_{V\_offset0} + \sigma^2_{V\_PVT}$$

($\sigma_{V\_offset0}$ is extracted from simulation data)

Input Common-Mode Voltage

- Input common-mode voltage is fluctuated
- Standard deviation of calibration code is σ_{Code}

$$\text{Error due to } V_{eff} = \frac{\partial V_{in\_diff\_cal}}{\partial V_{in\_com}} \times \Delta V_{in\_com}$$

$$= \frac{\Delta V_{eff}}{C}\left(1+\frac{\lambda}{2}\left(V_{dd}-V_{eff}\right)\right)\times\left(C_{on}-C_{off}\right)\sigma_{Code}$$

$$\text{Error due to } \lambda = \frac{V_{eff}}{C}\times\left(V_{dd}-V_{eff}\right)\frac{\Delta\lambda}{2}\times\left(C_{on}-C_{off}\right)\sigma_{Code}$$

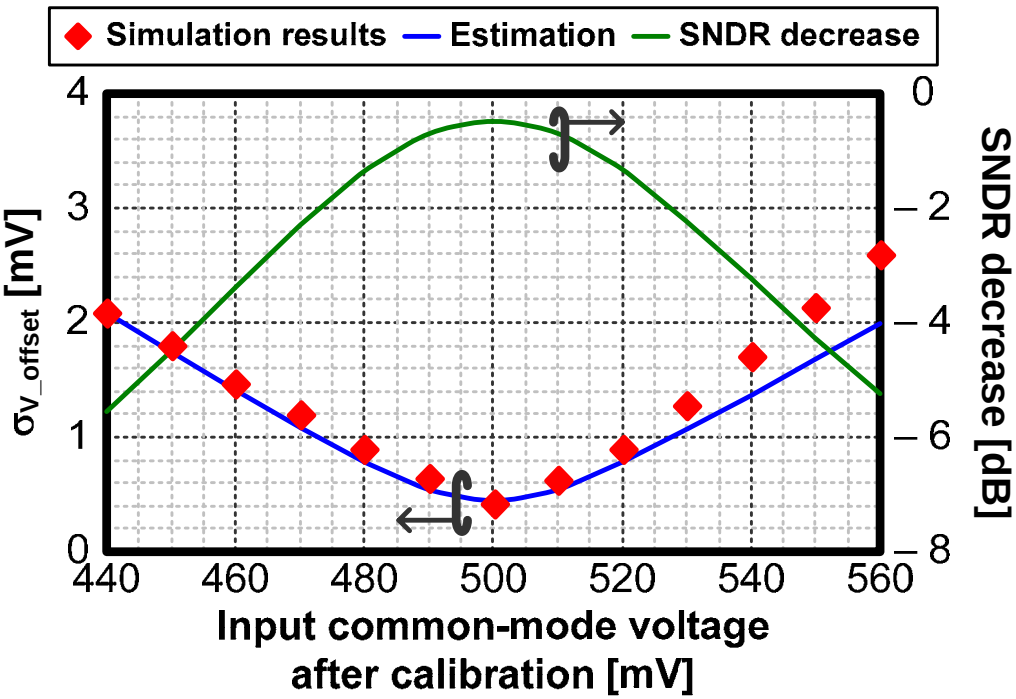
$$\text{Error due to } \left(V_{dd}-V_{eff}\right) = -\frac{V_{eff}}{C}\times\frac{\lambda}{2}\Delta V_{eff}\times\left(C_{on}-C_{off}\right)\sigma_{Code}$$

$$\sigma_{V\_PVT\_VCOM} = \frac{V_{eff}}{C}\left(1+\frac{\lambda}{2}\left(V_{dd}-V_{eff}\right)\right)$$

$$\times\sqrt{\left(\frac{\Delta V_{eff}}{V_{eff}}-\frac{\lambda\Delta V_{eff}}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2+\left(\frac{\left(V_{dd}-V_{eff}\right)\Delta\lambda}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2}\times\left(C_{on}-C_{off}\right)\sigma_{Code}$$

Simulation Results

- Calibration is conducted when V_{dd} is 1.0 V, V_{in_com} is 0.5 V, and *Temp* is 27 °C

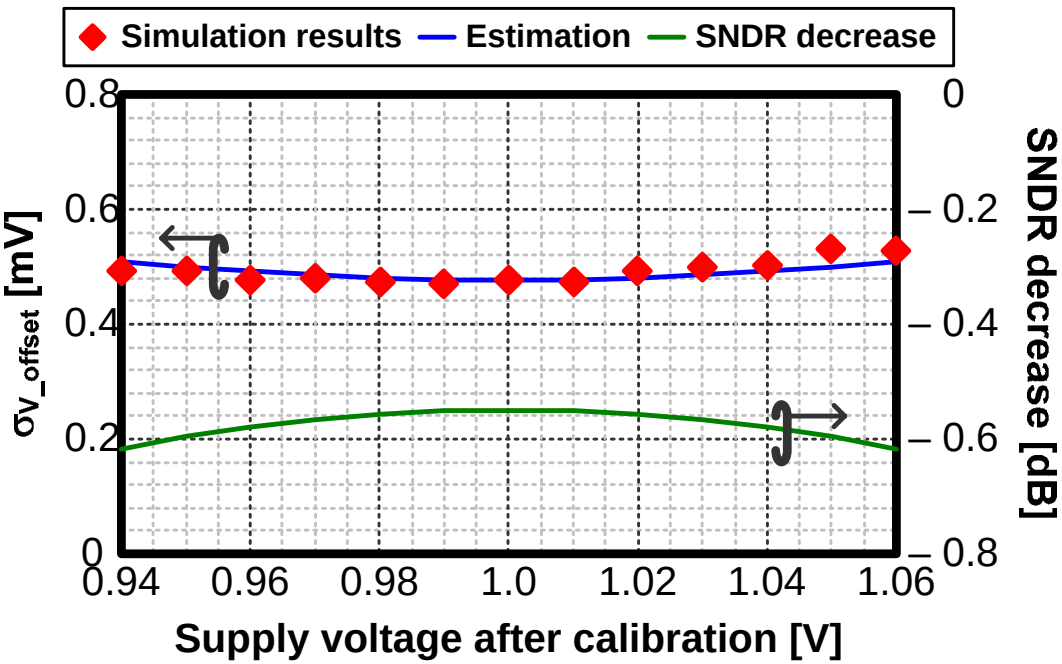


$$\mathrm{SNDR}_{\mathrm{decrease}} = \mathrm{SNDR} - \mathrm{SQNR} = -10\log\left(1+\frac{12}{V_{\mathrm{q}}^2}\sigma_{\mathrm{V}}^2\right)$$

Fig. Influence of input common-mode voltage on the capacitance calibration (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).

Influence of Supply Voltage

- Calibration is conducted when V_{dd} is 1.0 V, V_{in_com} is 0.5 V, and *Temp* is 27 °C

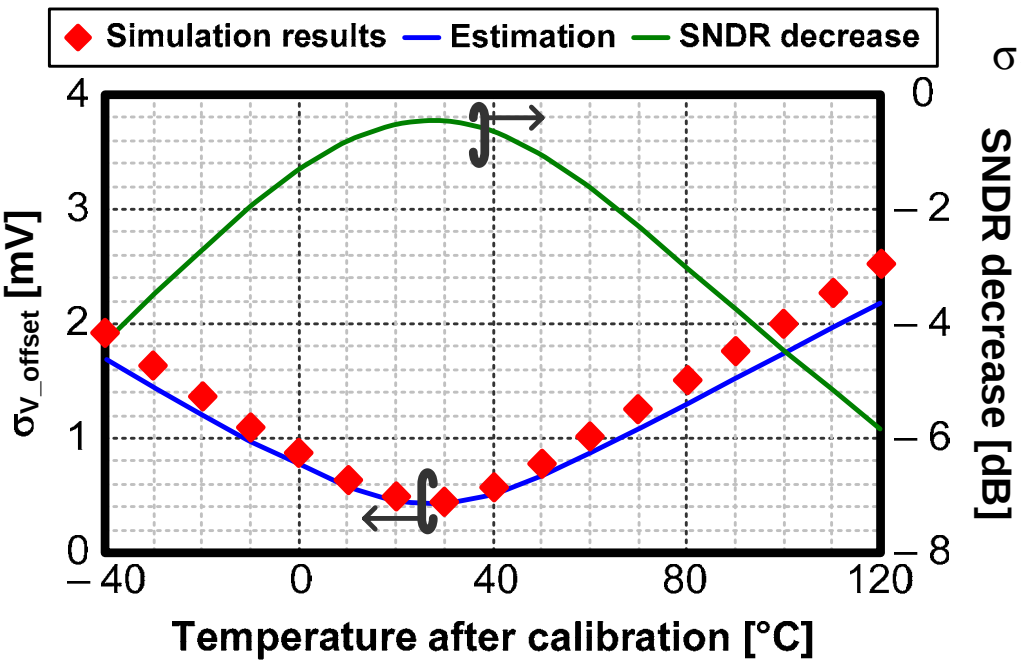


$$\sigma_{V\_PVT\_Vdd} = \frac{V_{eff}}{C} \times \left(1 + \frac{\lambda}{2}\left(V_{dd} - V_{eff}\right)\right) \times \sqrt{\left(\frac{\lambda \Delta V_{dd}}{2 + \lambda\left(V_{dd} - V_{eff}\right)}\right)^2} \times \left(C_{on} - C_{off}\right)\sigma_{Code}$$

Fig. Influence of supply voltage on the capacitance calibration (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).

Influence of Temperature

- Calibration is conducted when V_{dd} is 1.0 V, V_{in_com} is 0.5 V, and *Temp* is 27 °C



$$\sigma_{V\_PVT\_T} = \frac{V_{eff}}{C}\times\left(1+\frac{\lambda}{2}\left(V_{dd}-V_{eff}\right)\right)\left(\left(-\frac{\Delta V_{th}}{V_{eff}}+\frac{\lambda\Delta V_{th}}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2+\left(\frac{\left(V_{dd}-V_{eff}\right)\Delta\lambda}{2+\lambda\left(V_{dd}-V_{eff}\right)}\right)^2\right)^{\frac{1}{2}}\times\left(C_{on}-C_{off}\right)\sigma_{Code}$$

Fig. Influence of temperature on the capacitance calibration (1 LSB = 4.5 mV and a number of the Monte Carlo simulation is 500).

Conclusions

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- A **pseudo-differential dynamic comparator** with load capacitance calibration is analyzed
  - The **gain** of a dynamic amplifier
    - Expressed by **a ratio of V_{dd} to V_{eff} and λ** of an input transistor
    - Gain is inversely proportional to V_{eff}
  - Thermal noise, **input-referred compensate voltage**, and influence of **PVT variation** are analyzed
    - A dynamic comparator is **sensitive to PVT variation**
      - Mainly decided by V_{eff}

Acknowledgements

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